REMARKS / ARGUMENTS

The present application includes pending claims 1-50. Claims 7-13, 15, 21-27, 30-34, 38-48, and 50 are rejected. Claims 14, 28-29, 35-37, and 49 have been objected to.

By this Amendment, claims 1-6, 14, 16-20, 28-29, 35-37, and 49 have been cancelled, claims 7, 40, and 42-44 have been amended, and new claims 51-57 have been added. The Applicant respectfully submits that the claims define patentable subject matter.

Claims 7-13, 15, 40-48, and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,452,235, issued to Isani (hereinafter, Isani), in view of U.S. Patent No. 5,812,144, issued to Potu et al. (hereinafter, Potu). Claims 21-27, 30-34, and 38-39 are rejected as being unpatentable over Potu.

The Applicant respectfully traverses these rejections at least based on the following remarks.

REJECTION UNDER 35 U.S.C. § 103

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure ("MPEP") states the following:

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the teaching. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

See MPEP at § 2142, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) (emphasis added). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art suggests the desirability of the combination," and that "although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be *a suggestion or motivation in the reference* to do so'" (citing In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990)). Moreover, MPEP § 2143.01 also states that the level of ordinary skill in the art cannot be relied upon to provide the suggestion...," citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 USPQ 2d 1161 (Fed. Cir. 1999). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness.

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

I. THE PROPOSED COMBINATION OF ISANI AND POTU DOES NOT RENDER CLAIMS 7-13, 15, 40-48, AND 50 UNPATENTABLE

The Applicant now turns to the rejection of claims 7-13, 15, 40-48, and 50 as being unpatentable over Isani in view of Potu.

A. Independent Claims 7 and 40

With regard to the rejection of independent claim 7 under 103(a), the Applicant submits that the combination of Isani and Potu does not disclose or suggest at least the limitation of "clock-selection circuitry that receives a video input clock and a display output clock and selects one of the video input clock and the display output clock for upscaling and one of the video input clock and the display output clock for downscaling of the video image," as recited by the Applicant in independent claim 7.

The Final Office Action concedes the following:

> However it is noted that Isani fails to disclose capable of both downscaling the video image to generate a first scaled video image and upscaling the video image to generate a second scaled video image, the scaler engine using a clock selected between a video input clock and a display output clock; and means for determining whether the video image is to be downscaled or upscaled.

See the Final Office Action at page 3. To address the deficiencies of Isani, the Examiner seeks support in Potu, and states the following:

> Potu discloses capable of both downscaling the video image to generate a first scaled video image and upscaling the video image to generate a second scaled video image (col. 5, lines 43-56), using a clock selected between a video input clock and a display output

> clock (col. 5, lines 50-52); and means for determining whether the video image is to be downscaled or upscaled (col. 5, lines 5-7).

See id. Initially, the Applicant points out that the video adapter 22 of Potu performs on-the-fly resizing without requiring separate scaling chip. *See* Potu, col. 5, lines 49-53. In other words, **Potu does not disclose a video scaler or a scaler engine, and the video processing functionalities of Potu do not relate to a video scaler or a scaler engine**, as recited in Applicant's claim 7.

The Applicant points out that **neither Isani nor Potu disclose any circuitry that receives and selects between a video input clock and a display output clock for purposes of upscaling or downscaling a video image**. With regard to Applicant's limitation of selecting between a video input clock and a display output clock, the Examiner seeks support in the following citation of Potu:

> What video adapter 22 provides is the ability to perform on-the-fiy resizing with pixel clock manipulation 50 of time-interleaved digital video component YVV data without requiring a separate scaling chip, additional buffers, or associated interface logic.

See Potu, col. 5, lines 50-52. The Applicant is confused as to why the Examiner is using this citation since col. 5, lines 50-52, as well as the remaining portion of Potu, does not disclose or suggest a display output clock and a video input clock, as well as receiving and selecting between the display output clock and the video input clock. In fact, Potu does not disclose of any clock signal selection by the video adapter 22.

Therefore, the Applicant maintains that the combination of Isani and Potu does not disclose or suggest at least the limitation of "clock-selection circuitry that receives a video input clock and a display output clock and selects one of the video input clock and the display output clock for upscaling and one of the video input clock and the display output clock for downscaling of the video image," as recited by the Applicant in independent claim 7.

Furthermore with regard to the rejection of independent claim 7 under 103(a), the Applicant submits that the combination of Isani and Potu does not disclose or suggest at least the limitation of "means for determining whether the video image is to be downscaled or upscaled," as recited by the Applicant in independent claim 7. With regard to Applicant's limitation of "means for determining whether the video image is to be downscaled or upscaled," the Examiner seeks support in the following citation of Potu:

> Synchronization signals from video decoder 40 are also forwarded to field memory 46 through either field memory write and downscale logic 46A or field memory read and upscale logic 46B.

See Potu, col. 5, lines 5-7. The Applicant is confused as to why the Examiner is using this citation since col. 5, lines 5-7, as well as the remaining portion of Potu, does not disclose or suggest "means for determining whether the video image is to be downscaled or upscaled," as recited in Applicant's claim 7. In fact, Potu does

not disclose of any determination of whether an image is to be upscaled or downscaled by the video adapter 22.

The Examiner also states the following in the Final Office Action:

> In response, Potu discloses receiving video information (col. 4, ll. 45-50) and storing the video information in field memory "46" having both upscale logic "46B" and downscale logic "46A". **Potu teaches providing synchronization signals to determine which field memory logic is to store the data (col. 5, ll. 4-7, 10-15)**, where the field memory both provides the data to be scaled (col. 5, ll. 35-40) and stores the data that is scaled (col. 6, ll. 22-24). Thus, Potu discloses means for determining whether the video image is to be downscaled or upscaled as he teaches providing synchronization signals that determine whether the data is to be stored as upscaled or downscaled.

See the Final Office Action at page 12 (emphasis added). The Applicant respectfully disagrees, especially with the above bolded statement. At col. 5, lines 4-7 and 10-15, Potu simply discloses that synchronization signals are forwarded from the video decoder 40 to field memory 46 via logic 46A or 46B. Potu does not disclose "providing synchronization signals to determine which field memory logic is to store the data," as stated by the Examiner. In fact, Potu is silent as to any determination with regard to performing downscaling or upscaling relating to logic 46A and 46B.

Therefore, The Applicant maintains that the combination of Isani and Potu does not disclose or suggest at least the limitation of "means for determining

whether the video image is to be downscaled or upscaled," as recited by the Applicant in independent claim 7.

Accordingly, the proposed combination of Isani and Potu does not render independent claim 7 unpatentable, and a *prima facie* case of obviousness has not been established. Independent claim 40 is similar in many respects to the method disclosed in independent claim 7. Therefore, the Applicant submits that independent claim 40 is also allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 7.

B. Rejection of Dependent Claims 8-13, 15, 41-48, and 50

Based on at least the foregoing, the Applicant believes the rejection of independent claims 7 and 40 under 35 U.S.C. § 103(a) as being unpatentable over Isani in view of Potu has been overcome and requests that the rejection be withdrawn. Additionally, claims 8-13 and 15 depend from independent claim 7, and claims 41-48 and 50 depend from independent claim 40. Therefore, claims 8-13, 15, 41-48, and 50 are, consequently, also respectfully submitted to be allowable.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 7-13, 15, 40-48, and 50.

II. ISANI AND POTU CANNOT BE COMBINED

The Examiner is referred to M.P.E.P. § 2145(X)(D)(2), which clearly states that "**[i]t is improper to combine references where the references teach away from their combination.**" As already stated above, Isani discloses the use of a video scaler. Furthermore, Potu discloses performing on-the-fly resizing without requiring separate scaling chip. *See* Potu, col. 5, lines 49-53. In other words, **Potu does not disclose a video scaler or a scaler engine, and the video processing functionalities of Potu do not relate to a video scaler or a scaler engine**, as recited in Applicant's claim 7.

Therefore, Potu teaches away from Isani (since it specifically teaches away from the use of a video scaler), thereby teaching away from the combination of Isani and Potu. See, e.g., M.P.E.P. § 2145(X)(D)(2). Accordingly, Isani cannot be properly combined with Potu. Since Isani cannot be properly combined with Potu, the Examiner cannot maintain an obviousness rejection of claims 7-13, 15, 40-48, and 50 based on the combination of Isani and Potu.

The Applicant respectfully submits that Isani and Potu were improperly combined.

III. Potu Does Not Render Claims 21-27, 30-34, and 38-39 Unpatentable

The Applicant now turns to the rejection of claims 21-27, 30-34, and 38-39 as being unpatentable over Potu.

A. Independent Claims 21 and 30

With regard to the rejection of independent claim 21 under 103(a), the Applicant submits that Potu does not disclose or suggest at least the limitation of "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

The Final Office Action states the following:

> Regarding claim 21, Potu discloses receiving a video image by a video scaling engine (col. 4, ll. 44-50); reducing memory space by scaling the video image before writing the video image to memory or after reading the video image from the memory (i.e. logic for determining whether to write the data to memory and downscale or read the data from memory and upscale, which provides for a reduction in bandwidth of the input data, which in turn requires less memory space as the reduction of data uses less memory space for storage) (col. 5, ll. 4-7, 10-15,43-45); and scaling the received video image based on the determination (col. 5, ll. 28-31; col. 6, ll. 22-24).

See the Final Office Action at pages 6-7. The Applicant respectfully disagrees. The Applicant points out that **Potu does not disclose any video scaling engine. In fact, as already explained above, Potu teaches away from the use of a video scaler**.

Furthermore, the Examiner relies on col. 5, lines 4-7, 10-15, and 43-45 of Potu for support. The Applicant is confused as to why the Examiner is citing to col. 5, lines 4-7, 10-15, and 43-45 of Potu since this citation, as well as any of the remaining portion of Potu, does not disclose any details as to how scaling is performed. More specifically, Potu does not disclose or suggest "determining whether the video scaling engine requires less memory space to scale the video image before writing the video image to memory or after reading the video image from the memory," as recited by the Applicant in independent claim 21.

Accordingly, Potu does not render independent claim 21 unpatentable, and a *prima facie* case of obviousness has not been established. Independent claim 30 is similar in many respects to the method disclosed in independent claim 21. Therefore, the Applicant submits that independent claim 30 is also allowable over the references cited in the Final Office Action at least for the reasons stated above with regard to claim 21.

B. Rejection of Dependent Claims 22-27, 31-34, and 38-39

Based on at least the foregoing, the Applicant believes the rejection of independent claims 21 and 30 under 35 U.S.C. § 103(a) as being unpatentable over Potu has been overcome and requests that the rejection be withdrawn. Additionally, claims 22-27 depend from independent claim 21, and claims 31-34

and 38-39 depend from independent claim 30. Therefore, claims 22-27, 31-34, and 38-39 are, consequently, also respectfully submitted to be allowable.

The Applicant also reserves the right to argue additional reasons beyond those set forth above to support the allowability of claims 22-27, 31-34, and 38-39.

IV. New Claims 51-57

New claims 51-57 correspond to the objected to claims 14, 28-29, 35-37, and 49. Therefore, the Applicant submits that no new matter has been added by claims 51-57, and claims 51-57 are allowable.

CONCLUSION

Based on at least the foregoing, the Applicant believes that all claims 7-13, 15, 21-27, 30-34, 38-48, and 50-57 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Attorney at (312) 775-8176.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously solicited.

Respectfully submitted,

Date: 05-DEC-2007

/Ognyan I. Beremski/

Ognyan Beremski, Esq.
Registration No. 51,458
Attorney for Applicant

McAndrews, Held & Malloy, Ltd.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(312) 775-8000

/ OIB